QuTech

# Spin-2+ QPU

## Spin-based Quantum Processor Unit

The number of quantum computing use cases in the field of quantum simulations, optimization, and machine learning is steadily increasing. At QuTech we are convinced that offering the public broad access to technologies such as quantum computing hardware as well as a quantum computing simulator tool will further stimulate this growth. Therefore, Quantum Inspire (QI) was launched on April 20, 2020. At that time, this was one of the most advanced solid state quantum chips based on single-electron spins and the only one in the world available for public online access [1].

This time we provide online access to a highly upgraded version, **Spin-2+**. This device uses a linear array of six quantum dots. Spin-2+ utilizes the left three dots to define one ancilla qubit in dot 1 and two data qubits in dots 2 and 3. The readout of the two data qubits is enabled via the ancilla qubit, based on spin-blockade relying on Pauli exclusion.

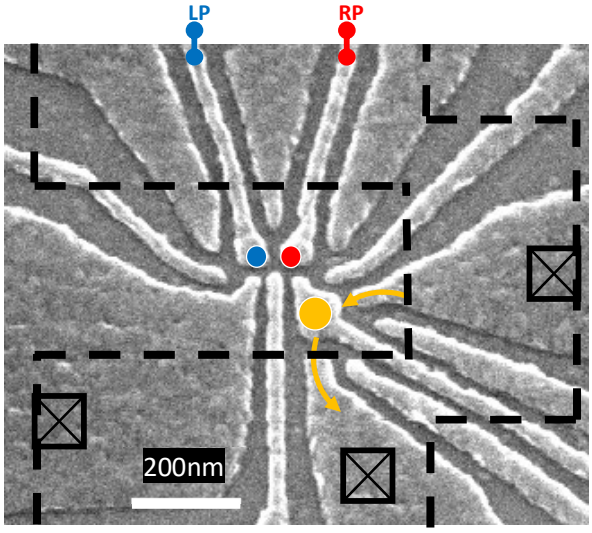


*Figure 1 SEM picture of the 2020 Spin-2 QPU (2D1S Gen 0 design). A single-layer, 2-qubit QPU based on isotopically purified Si/SiGe heterostructure, with 2 quantum dots and one sensing dot. Left plunger (LP blue), Right plunger (RP red) and Sensing Dot (SD yellow).*

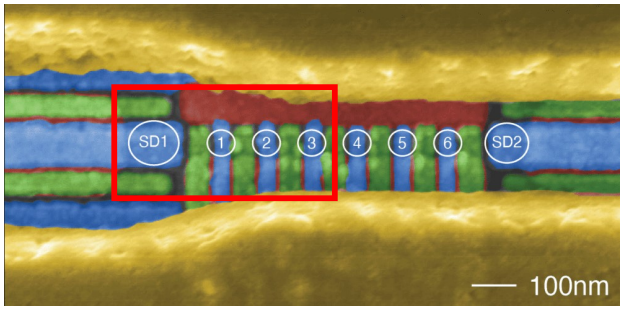


*Figure 2 False colored SEM picture of the 2024 **Spin-2+ QPU** (6D2S Gen 1 design). A multi-layer gate stack, defining a linear array of six quantum dots 1 to 6 on our in-house grown SiGe/$^{28}$Si/SiGe heterostructure (4-6). Spin-2+ utilizes the left three dots and Sensing Dot 1 (SD1) to define one ancilla qubit in dot 1 and two data qubits in dots 2 and 3. PSB readout through the ancilla qubit is used to readout the two data qubits. Static and dynamic potentials are defined by the screening gates (red), barrier gates (green) and plunger gates (blue).*

Our Spin-2+ QPU is a 2-qubit programmable quantum processor based on spin qubits in Silicon, kept at a temperature of 200 mK inside a dilution refrigerator. Conventional DC-carrying cables and high frequency transmission lines bring the signals to and from the Spin-2+ QPU. Single-electron spins trapped in semiconductor quantum dots are particularly promising building blocks of a quantum processor [2,3]. These devices can be manufactured and tailored by standard lithographic techniques such as e-beam and EUV, which is a considerable advantage for potential future large-scale integration of many qubits. In addition, they are controlled and read out by current-state electronics and are promising for very large-scale integration thanks to their small size and similarity to classical transistor technology. The ancilla qubits 1 (and 6) used for PSB readout have 3 electrons, which increases the readout window by creating an orbit-like splitting.

**Quantum Inspire Spin-2+ QPU FACT SHEET**

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## Performance of Spin-2+ QPU

*Table 1 Key performance parameters of Spin-2 (left) and Spin-2+ (right). (q0) / q1 / q2 : (dot1) / dot2 / dot3*

| ***Key performance parameters*** | *Spin-2* | ***Spin-2+*** |
|---|---|---|
| ***Material*** | Si-28 in a @@ nm QW in SiGe | **Si-28 in a 6 nm QW in SiGe** |
| ***Single qubit gate control*** | EDSR microwave pulsing | **EDSR microwave pulsing** |
| ***Two-qubit gate control*** | Exchange interaction | **Exchange interaction** |
| ***Read-out method (spin to charge conversion)*** | Spin-selective tunnelling | **Pauli Spin Blockade (PSB)** |
| ***Visibility*** | ~ 80% | (98%) **/ 97% / 89%** |
| ***Energy relaxation time T1*** | > 20 ms (similar device) | (280) **/ 181 / 261 ms** |
| ***Phase coherence time T2**** | > 6 µs | (3,4) **/ 1,5 / 6,4 µs** |
| ***Phase coherence time $T2^{Hahn}$*** | --- | (15,8) **/ 8,4 / 11,6 µs** |
| ***Single-qubit gate (X90) fidelity*** | ~ 99,0% (avg per qubit) | (99,8%) **/ 99,8% / 99,9%** |
| ***Two-qubit gate (CZ) fidelity*** | 90,0% | **95,5%** |
| ***Qubit state preparation & readout fidelity*** [1] | ~ 85% (avg per qubit) | (96%) **/ 98% / 97%** |
| ***Single-qubit gate (X90) duration*** | 250 ns | (84) **/ 56 / 84 ns** |
| ***Two-qubit gate(CZ) duration*** | 150 ns | **300 ns** |
| ***Readout duration (full register)*** | 2 x 300 µs = 600 µs | **100 µs** |
| ***PSB integration time*** | n.a. | **37 us** |

The key performance parameters of Spin-2+ are given in table 1. Notably, Spin-2+ demonstrates (relative to Spin-2):

- improved visibility: from 80% to 95% on average
- improved single-qubit gate fidelity: from 99,0% to 99,8%
- improved two-qubit gate fidelity: from 90% to 95,5%
- improved qubit state preparation and readout fidelity: from 72% to 97%
- improved single-qubit gate duration: from 250 ns to <90 ns
- improved qubit register readout duration: from 600 µs to 100 µs, at a single PSB readout duration of 37 µs

Our system uses virtual Rz gates and X90 gates to create arbitrary single-qubit operations. On average one X90 gate is used to create single-qubit Clifford gates. Two X90 gates are required to create non-Clifford single-qubit gates (F = 99,7%). Figure 3 shows the measured resonance frequencies at the applied external magnetic field of 80 mT. Only qubits q0, q1 and q2 are used in Spin-2+ due to the insufficient frequency spacing between the other qubits, resulting in too much cross talk between q3, q4 and q5 to make them useful as computational qubits.

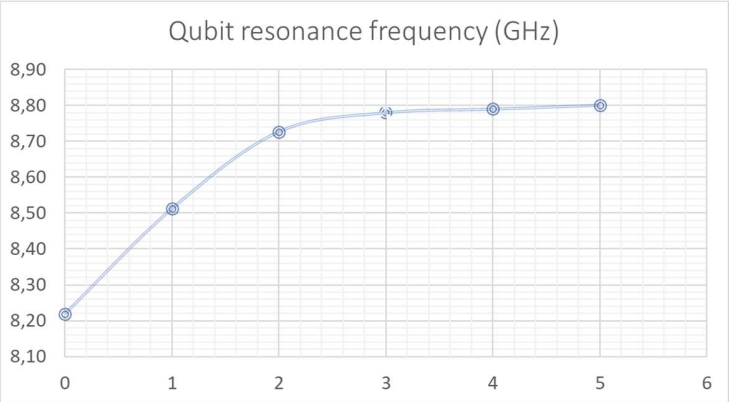



*Figure 3 Qubit resonance frequencies at the applied external magnetic field of 80 mT. At this magnetic field, the resonance frequency of q3 was not determined. The value plotted is interpolated based on measured values at a different magnetic field.*

[1] Benchmark method used does not distinguish state preparation from measurement errors.

**Quantum Inspire Spin-2+ QPU FACT SHEET**

## Development of Spin-2+ QPU

The Spin-2+ QPU developed at QuTech is based on a six-qubit device using electron spins in silicon [4,5], of which three are used. Two of them are the data qubits allowing for arbitrary single-qubit rotations and two-qubit gates. The remaining qubit is the ancilla qubit allowing for Pauli spin blockade (PSB)-readout via an additional single-electron-transistor charge sensor nearby. The six qubits are hosted in an electrostatically defined linear array of six quantum dots realized in low-disorder, isotopically purified $^{28}$Si/SiGe heterostructures [6,7]. Single and two-qubit gates are implemented by applying microwave and DC pulses to the electrodes which electrostatically define the quantum dots and a micromagnet which enables electric-dipole spin resonance and individual addressing of the qubits. More details on the functional requirements and the device lifecycle including materials, fabrication and electrical screening can be found in Figure 2 and in references [4, 5].

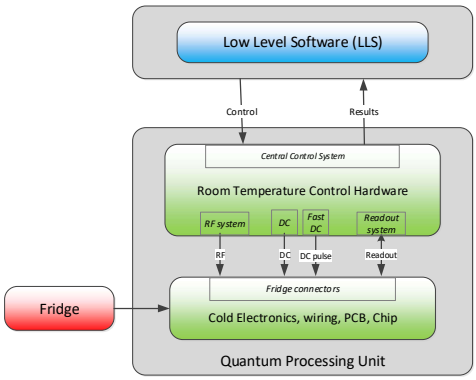
## Spin-2+ control stack


The PCB with QPU is placed inside a dilution fridge, cooling down the sample to approximately 200 mK. Room Temperature control electronics and electronics inside the fridge (mainly for signal attenuation and filtering) is used to create the DC, AC and MW signals required to control and readout the qubits. Low Level Software (LLS) is used to convert the quantum instructions into micro-instructions for the hardware and to allow for accurate calibration and tuning of the system.

The QPU is wire-bonded to a PCB. This PCB, mounted on the cold finger of the fridge, is the interface between the fridge wiring carrying all control signals) and the QPU.

The room temperature control hardware consists of:

- Stable DACs to create a DC landscape to confine quantum dots
- AWGs to tune the DC landscape to steer quantum dots and to create the I/Q signals for up-converting
- Readout modules to initialize and readout the qubits
- Microwave source, mixing I/Q signals with a Local Oscillator (LO) signal to create the MW signals for qubit driving

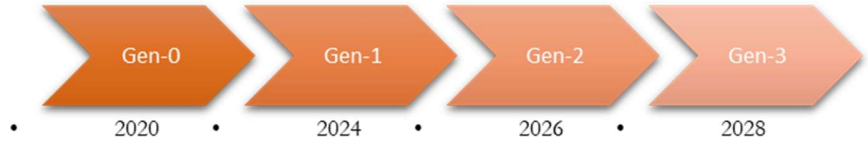



The control software of Spin-2+ makes use of building blocks from QuTech and its ecosystem [8]. It offers a generic environment to define, execute and analyze the whole range of required experiments from low level, e.g. simple scans, to high level, e.g. parametrized quantum circuits. It contains a library of generic experiment implementations that are required for autonomously keeping the system calibrated. These experiments consist of a measurement part and an analysis part (to retrieve system parameters from the measurement result). The system parameters are stored in a run-time database that contains all the information needed for executing calibrated quantum algorithms.

A calibration framework provides the configurable logic to organize the calibration experiments. It needs to balance the conflicting demands of requiring minimal system time versus ensuring maximal quantum performance. In general the strategy is to do quick measurements to check if calibration parameters are still valid and to only execute long experiments for parameters that require recalibration. In practice this can become quite complex due to dependencies between experiments and discontinuous changes in device characteristics. The configurable logic allows to tailor this process for each specific device. For the Spin-2+ system this ensures that it remains calibrated without human intervention for >24h.

## Future outlook

Spin-2 was our first Gen-0 device. With Spin-2+ we are launching a new Gen-1 architecture that extends the linear array to multiple dots. We also include a new spin-discrimination method that allows for faster and better read-out and which is also compatible with read-out and discrimination methods that will reach even higher fidelities, allow for multiplexed readout and scale beyond linear arrays.




Our future Gen-2 and Gen-3 architectures that are currently being designed, manufactured and tested, will aim for higher numbers of qubits, higher fidelities, extension beyond linear arrays to improve scalability and improve compatibility with multiplexed control and readout, integration of vertical interconnects and dense arrays of dots.

## References

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